



# Channel Temperature Model for Microwave AlGaN/GaN HEMTs on SiC and Sapphire MMICs in High Power, High Efficiency SSPAs

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## ABSTRACT

A key parameter in the design trade-offs made during AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs development for microwave power amplifiers is the channel temperature. An accurate determination can, in general, only be found using detailed software; however, a quick estimate is always helpful, as it speeds up the design cycle. This paper gives a simple technique to estimate the channel temperature of a generic microwave AlGa<sub>N</sub>/Ga<sub>N</sub> HEMT on SiC or Sapphire, while incorporating the temperature dependence of the thermal conductivity. The procedure is validated by comparing its predictions with the experimentally measured temperatures in microwave devices presented in three recently published articles. The model predicts the temperature to within 5 to 10 percent of the true average channel temperature. The calculation strategy is extended to determine device temperature in power combining MMICs for solid-state power amplifiers (SSPAs).

## I. INTRODUCTION

At the present time many research groups are studying AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs for high frequency (up to Ka-band), high power microwave applications [1–4]. The large RF power density generated in these amplifiers causes considerable self-heating, and a reasonably accurate estimate of the channel temperature is often desired. Knowledge of the temperature is essential as both the carrier mobility and reliability suffer. The mobility reduces with increasing temperature as  $(1/T)^{2.3}$ , with resulting decrease in DC and RF performance [5]. Both short and long term reliability are key parameters, which also reflect the need to rapidly calculate the temperature profile in a particular design.

Both the long and short period output power changes measured in many devices under stress testing are related to the device temperature. The trade-off in the number of fingers in a MMIC cell is controlled to some extent by the thermal hot spots that develop near the edge of the gate in the gate-drain access regions in the center of a cell. Several 2- and 3-D simulators [6–9] are available to determine temperature profiles. A 2-D electro-thermal package, MINIMOS-NT [10] considers the coupling between the current and heat transport equations, and thereby performs a self-consistent calculation. The SILVACO [11] suite of software also performs self-consistent calculations. A few recent articles [12–14] give techniques to quickly ascertain junction temperatures under certain conditions; two of which neglect the temperature dependence of the thermal conductivity. This article demonstrates a procedure to estimate the channel temperature in microwave AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs on either SiC or Sapphire, using simple analytic expressions, which includes the change in thermal conductivity with temperature. The device is modeled using the thermal resistance method, and is applicable to multi-gate, multi-material, structures, and a wide range of power dissipation levels.

We do not want to mislead the reader into thinking we have a nearly final answer to the many problems that plague AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs (such as current collapse, permanent electrical change after initial electrothermal stress, etc.). What we demonstrate is the reasonably accurate temperature estimate by using the quiescent dissipated power. This is a contribution in lieu of the extreme difficulty in modeling the device accurately using existing software. As stated in [13] the electrothermal modeling of devices is such a difficult problem that the present models (circa 2001) are either oversimplified or rather inefficient from a computational point of view. For example, Wachutka [15] developed the first rigorous specification of heat generation in a semiconductor based on thermodynamic concepts. This model is available with the SILVACO [11] package, whereas the simpler expression,  $H = \bar{J} \cdot \bar{E}$  is also available to reduce complexity and simulation time. Efficient thermal management of electronic components is essential to minimize the influence of thermomechanically induced stress and thermal load. The fact that the 2D-electron gas in AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs is about 50 percent supported by piezoelectric polarization due to mechanical strain; the interaction of temperature, strain, piezoelectric fields, and carrier densities at critical positions

in the device is of paramount importance. Here we take a less exact approach to demonstrate the application of simple formulas for the analysis of combined devices used for solid state power amplifiers (SSPAs). We do not attempt to ascertain the complex interaction in a power device, just the average temperature to determine reasonable spacing between electrically combined devices as well as the package layout.

## II. ANALYSIS PROCEDURE

A generic microwave power AlGaIn/GaN HEMT layout and its cross section are shown in figures 1 and 2, respectively. Being a power device it has a multi-finger gate structure, and the die is attached to a Cu-tungsten heat sink for efficient thermal management. The thermal conductivities for the many material layers in the cross-section were determined by making rough averages of the values reported in the literature. To convert the actual device depicted in figures 1 and 2, into one wherein analytical formulas are available, we use the following approach. On the left in figure 3 we have shown an equivalent effective heat aperture to model the heat generated on the top surface (primarily in the gate-drain access regions). Then on the right we show a series of thermal resistances which depend on the thermal conductivity and thickness of each layer of the device. In cases where the separation between the gate fingers is large with respect to the chip thickness, the heat source at the position we show as  $T_{\text{CHANNEL}}$  in the figure, is a thin strip of uniform heat generation, which is about the same physical size as the gate electrode, and located in the gate-drain access region. The technique consists of determining the thermal footprints of the heat sources at each successive lower layer, and then determining that layer's thermal resistance.

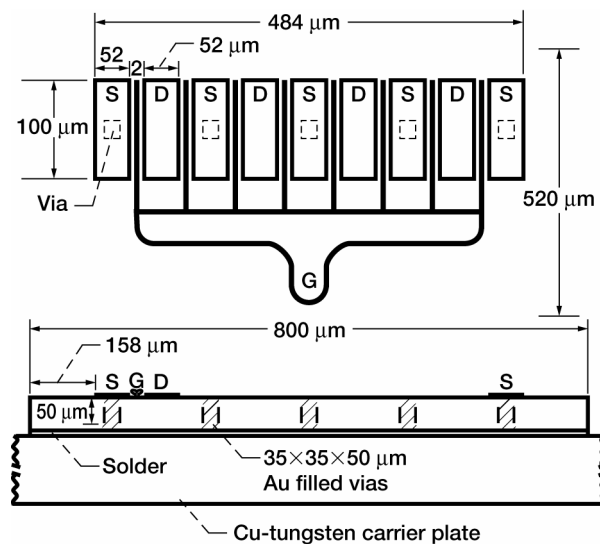


Figure 1.—Schematic of an 8 gate AlGaIn/GaN HEMT for a microwave power amplifier.

0.1-0.175 μm	Si <sub>3</sub> N <sub>4</sub> (passivation layer)	κ = 0.0096	
0.02 μm	GaN (cap layer)	κ = 1.6	
0.022 μm	Al <sub>0.2</sub> Ga <sub>0.8</sub> N (barrier layer)	κ = 1.6	
0.5 μm	GaN (buffer layer)	κ(T <sub>0</sub> ) = 1.6 κ(T) = calculated 2 deg*	
0.015 μm	AlN (nucleation layer)	κ = 0.1	
100 μm	SiC	Au source via κ = 3.18 κ(T <sub>0</sub> ) = 3.4 κ(T) = calculated 35 μm	
20 μm	AuSn AuGe Epoxy Silver epoxy	κ = 2.4 κ = 0.9 κ = 0.3-.6 κ = 0.016-.075	
1000 μm	Cu-tungsten (carrier)	κ = 4	

Note: The units for thermal conductivity κ are W/(cm-K)

\* Two dimensional electron gas

Figure 2.—Cross-section model of the HEMT device, showing approximate layers of material with average, or ranges, of thermal conductivities.

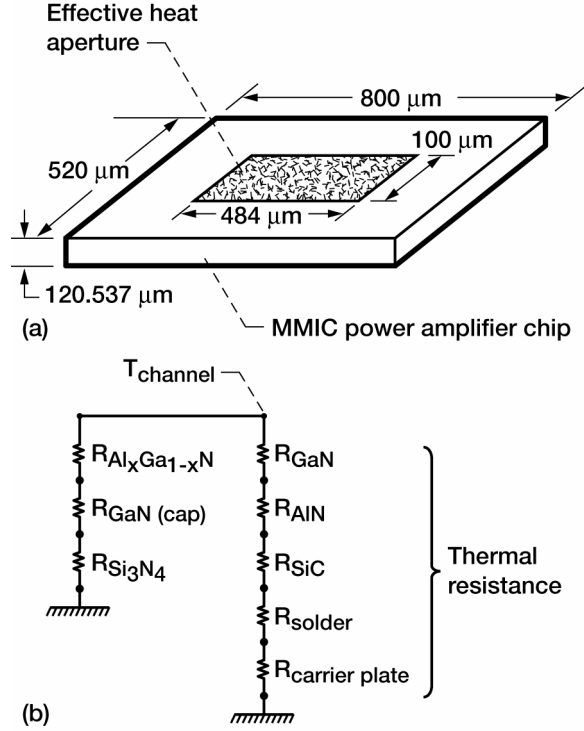


Figure 3.—(a) Equivalent heat source of the 8 gate HEMT device for modeling thermal profile. (b) Equivalent circuit model representation of the thermal resistances of the HEMT device.

#### A. Expressions for Temperature Dependent Thermal Conductivity

In principle, in any heat transport problem, one solves for the temperature field from the heat flow equation

$$\nabla \cdot \{ \kappa_i(T) \nabla T \} = -P \quad (1)$$

where  $\kappa_i(T)$  is the temperature dependent thermal conductivity in the  $i$ -th layer,  $T$  is the temperature in Kelvin, and  $P$  is the dissipated power density in  $\text{W/m}^3$ . The equation is altered by defining an equivalent artificial temperature via the Kirchhoff transformation

$$T_i^e = T_o + \frac{1}{\kappa_i(T_o)} \int_{T_o}^T \kappa_i(\xi) d\xi \quad (2)$$

where  $T_o$  is the reference temperature in K,  $T_i^e$  is the transformed temperature in the  $i$ -th layer, and  $T$  is the real temperature there in K. The transform linearizes equation (1) with the result

$$\kappa_i(T_o) \nabla^2 T_i^e = -P \quad (3)$$

While the Kirchhoff transform linearizes the heat equation, the nonlinearities inherent in equation (1) become a problem when layers of different materials are considered. When the layers have different functional relationships for their thermal conductivities  $\kappa_i(T)$ , then the transformed temperature across a boundary separating two

homogeneous regions will be discontinuous. Only when the ratio of the conductivities  $\kappa_i(T)/\kappa_{i+1}(T)$  is temperature independent, will the transformed temperature be continuous across the interface [16]. With this in mind, our first task is to determine analytical expressions for the temperature dependent thermal conductivities of the GaN, SiC, and Sapphire layers. We have not found an analytical expression for that of GaN which was developed from measured data, so we choose the following expression

$$\kappa_{\text{GaN}}(T) = 1.6 \left( \frac{300}{T} \right)^{1.4} \frac{\text{W}}{\text{cm} \cdot \text{K}} \quad (4)$$

This was arrived at by assuming GaN is sufficiently similar to GaP [17–18] (to choose the exponent), and the coefficient is in the range reported in the literature. For SiC we choose [19]

$$\kappa_{\text{SiC}}(T) = 3.4 \left( \frac{300}{T} \right)^{1.5} \frac{\text{W}}{\text{cm} \cdot \text{K}} \quad (5)$$

which was obtained from curve fits to experimental data. For Sapphire we assume [20]

$$\kappa(T) = \frac{73.9}{T - 159} \approx \frac{(0.49)(300)}{T} \frac{\text{W}}{\text{cm} \cdot \text{K}} \quad (6)$$

The first part of expression (6) was determined from curve fits of measured data, and the second one was an attempt to have a  $1/T$  variation. Figure 4 plots the above thermal conductivities. Observation of equations (4) to (6) shows that the ratios of the thermal conductivities are not independent of temperature, but they are not real strong functions of temperature. The change in the ratio for GaN on SiC is 5 percent over the temperature range of 300 to 500K. The corresponding change for GaN on Sapphire is 23 percent. This variability is not a problem as we determine the actual temperature at each interface at each step in the calculation. The variability becomes a problem when developing computational codes. We recognize that the leading coefficients and exponents are approximate as they are dependent on varying material parameters such as percent of cubic (Zincblende) phase in an otherwise hex (Wurtzite) phase sample. The dislocation densities, cracks, and other growth dependent factors will force changes in the formulas, but they are accurate enough for practical purposes.

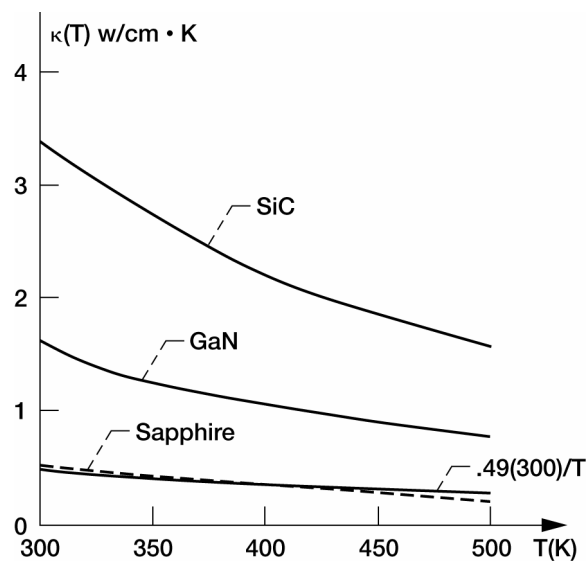


Figure 4.—The change in thermal conductivity versus temperature for SiC and sapphire substrates, and GaN epitaxial layers.



### B. Expressions for Thermal Resistance for Single Heat Source (Gate Finger)

The thermal resistance  $R_{TH}$  in (K/W) is determined by using the complete 3-D nature of the heat spreading. A device with a single gate finger can be modeled as a single heat source of length  $2l_x$  and width  $2l_y$  as shown in figure 5. The thermal resistance of any layer in the stack is given by [12].

$$R_{TH} = \frac{1}{\kappa} \int_0^w \frac{dz}{A(z)} = \frac{1}{4\kappa l_x} \frac{1}{(\gamma_e \tan \alpha - \tan \beta)} \ln \left[ \frac{l_x + w \tan \alpha}{l_x + w \frac{\tan \alpha}{\gamma_e}} \right] \left( \frac{K}{w} \right) \quad (7)$$

where

$$(\tan \alpha)_i = \left( 1 - l_{x_n} \right) \frac{w_n + \frac{\rho_s}{1 + \rho_s} l_{x_n}}{w_n + \frac{1}{1 + \rho_s} l_{x_n}} \bigg|_i \quad (8)$$

$$(\tan \beta)_i = \left( 1 - l_{x_n} \frac{\gamma_e}{\gamma_s} \right) \frac{w_n + \frac{\rho_s}{1 + \rho_s} l_{x_n} \gamma_e}{w_n + \frac{1}{1 + \rho_s} l_{x_n} \gamma_e} \bigg|_i \quad (9)$$

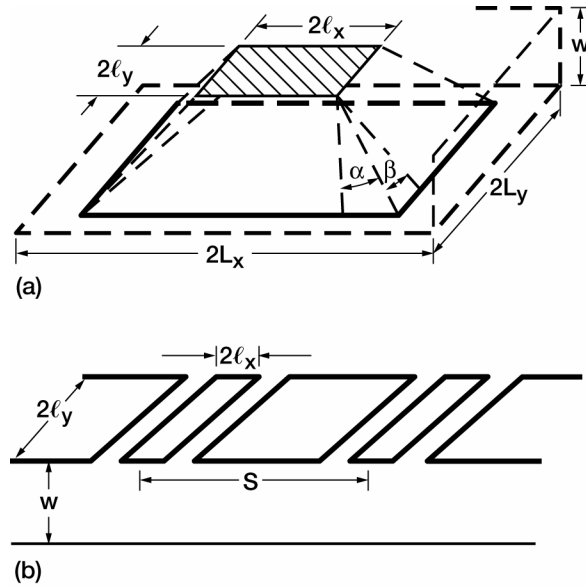


Figure 5.—Geometry for calculating thermal resistance for (a) a device with a single gate finger, (b) multi-gate structures.

where

$$w_n = \frac{w}{L_x} \quad (9a)$$

$$\gamma_e = \frac{l_y}{l_x} \quad (9b)$$

$$\gamma_s = \frac{L_y}{L_x} \quad (9c)$$

$$l_{x_n} = \frac{l_x}{L_x} \quad (9d)$$

$$\rho_s = \frac{\kappa_i}{\kappa_{i+1}} \quad (9e)$$

where the angles  $\alpha$  and  $\beta$ , the lengths  $L_x$  and  $L_y$ , and the thickness  $w$  are as shown in figure 5(a). This expression for  $R_{TH}$  is a general one, applicable to any layer in the resistance stack in figure 2.

### C. Expression for Thermal Resistance for Multiple Heat Sources (Multi-Gate Structures)

In a multi-gate structure there is a strong possibility that the fluxes will intersect. The thermal resistance of any layer in the stack is given by [21] (with typos corrected)

$$R_{TH} = \frac{\frac{n}{Z\kappa\pi}}{\left[ \frac{2(n-1)}{\ln M} - \frac{(n-2)}{\ln P} \right]} \quad (10)$$

where

$n$  the number of fingers  
 $Z$  total gate width =  $n(2l_y)$

and

$$M = \frac{2\sqrt{u} + 1}{\sqrt{u} - 1}, \quad u = \frac{\cosh \left[ \frac{\pi}{4} \left( \frac{S + 2l_x}{w} \right) \right]}{\cosh \left[ \frac{\pi}{4} \left( \frac{S - 2l_x}{w} \right) \right]} \quad (11)$$

$$P = 2 \sqrt{\frac{\cosh \left( \frac{\pi 2l_x}{4w} \right) + 1}{\cosh \left( \frac{\pi 2l_x}{4w} \right) - 1}} \quad (12)$$

The step-by-step procedure is as follows. Start with the heat sources on the top surface; which are stripes with the short side dimension being that of the gate length, or the gate-drain spacing. Using equations (8) and (9), determine the flow pattern as shown in figure 5(a). Use the room temperature values of  $\kappa$ , as the correct values to use are not yet available, since the temperature on the top surface is unknown at this point. Then the footprint on the next lower surface is determined. Continuing through all layers, one determines the thermal resistance stack. The calculation continues by starting at the assumed Cu-tungsten heat sink temperature and working upward through the layers. The change in temperature across a layer is given by

$$\Delta T_i = R_{TH_i} P_{DISS} \quad (13)$$

where  $P_{DISS}$  is the dissipated power in watts, i.e. the  $I_D V_D$  product,  $\Delta T_i$  = the temperature rise in K, and  $R_{TH_i}$  = the thermal resistance of the layer. The actual temperatures are used in the layers with constant thermal conductivity, and the artificial ones are determined in the GaN, SiC, and Sapphire layers. The actual temperature  $T_A$  at the surface of these materials is found from inverting the Kirchhoff transform, which yields

$$T_A(\text{GaN}) = \left\{ \frac{[T^e - T_o(3.5)](-0.4)}{T_o^{1.4}} \right\}^{-2.5} \quad (14)$$

$$T_A(\text{SiC}) = \left\{ \frac{[T^e - T_o(3)](-0.5)}{T_o^{1.5}} \right\}^{-2} \quad (15)$$

$$T_A(\text{Sapphire}) = T_o \exp \left[ \frac{T^e - T_o}{T_o} \right] \quad (16)$$

where  $T_o$  is the reference temperature, (the actual temperature at the lower surface of a given layer). With the first estimate of the channel temperature available, one may iterate using a more accurate value for  $\kappa(T)$ , rather than the room temperature value assumed. However, we find that this error reduction step is not usually needed. The procedure is now illustrated in detail in section III(A).

### III. COMPARISON WITH EXPERIMENTAL DATA

#### A. Single Gate Device on SiC

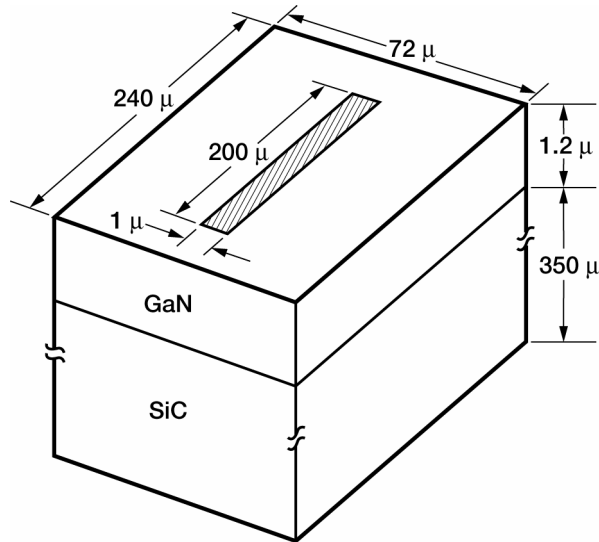


Figure 6.—Schematic of an equivalent heat source for a single gate device used in the measurement of the channel temperature by Raman spectroscopy [22].

For a device with a single gate of length  $2l_x = 1 \mu\text{m}$  and width  $2l_y = 200 \mu\text{m}$ , we model the heat source as a  $1 \times 200 \mu\text{m}$  stripe as shown in figure 6. We neglect the  $0.28 \mu\text{m}$  AlGaIn layer, because it is thin, and in [22] this was neglected in the calculation.

First steps: Calculate the thermal footprints at all material interfaces using equations (8) and (9). The  $1 \times 200 \mu\text{m}$  source region on the top of the GaN becomes a  $3.1 \times 200.2 \mu\text{m}$  source on the GaN/SiC interface. Using this we find that the footprint at the SiC/heatsink plane spreads to  $673 \mu\text{m}$  (which is greater than the  $72 \mu\text{m}$  dimension of the chip). Thus edge effects come into play, and may be handled using the techniques in [24]. We however, neglect these corrections, which we assume will be small in this particular case.

Next we determine the thermal resistance of the layers. Using equations (7) to (9) we find the first value for  $R_{TH}(\text{GaN})$  to be  $3.14 \text{ K/W}$ . We also use equation (10) with  $n = 1$ , and obtain  $R_{TH} Z \kappa = 0.587$ . Assume  $\kappa(T) = 1.6$  (again the  $300\text{K}$  value which we used in equations (7) to (9)) as we don't know the actual temperature and thus  $\kappa$  for that temperature. This will very slightly underestimate the final

channel temperature. We find  $R_{TH}(\text{GaN}) = 18.35 \text{ K/W}$ . Notice that this value is larger than the first value by a factor of 5.86. We assume this value is less reliable, and use the previously calculated one, i.e.  $R_{TH} = 3.14 \text{ K/W}$ . Using equations (7) and (8) we find the footprint on the SiC layer is  $3.1 \times 200.2 \text{ } \mu\text{m}$ . Use equation (10) again for this layer and obtain  $R_{TH}(\text{SiC}) = 29.72 \text{ K/W}$ . The dissipated power is  $1.754 \text{ W}$  which yields  $\Delta T(\text{SiC}) = 52 \text{ K}$ ,  $\Delta T(\text{GaN}) = 32.2 \text{ K}$ . Using equation (15) gives  $T(\text{SiC, actual}) = 86.6 \text{ }^\circ\text{C}$ . Then in the GaN layer,  $T^e = 359.6 + 32.2 = 391.8 \text{ K}$ , which is the modeled channel temperature,  $T_{\text{CHANNEL}}(\text{GaN, actual}) = 121 \text{ }^\circ\text{C}$ . In [22] and [23], temperature measurements on microwave AlGaIn/GaN HEMTs on both SiC or sapphire were made using Raman spectroscopy. The spatial resolution was  $1 \text{ } \mu\text{m}$  and the temperature accuracy was within  $10 \text{ }^\circ\text{C}$ . The measured value for the channel temperature  $T_{\text{CHANNEL}}$  was  $124 \pm 5 \text{ }^\circ\text{C}$ . The 3-D model used in [22] assumed a  $1/T$  variation in  $\kappa$  and predicted  $T_{\text{CHANNEL}} = 99 \text{ }^\circ\text{C}$ . The reason for the low accuracy is perhaps due to the assumed variation of  $\kappa$  with temperature. Thus our model achieves much better results than the 3-D model.

### B. Single Gate Device on Sapphire

For the sapphire substrate case we choose  $2l_x = 4 \text{ } \mu\text{m}$  (gate length),  $\kappa(\text{sapphire, } 300 \text{ K}) = 0.49$ ; then calculate  $R_{TH}(\text{GaN}) = 8.35 \text{ K/W}$ ,  $R_{TH}(\text{SiC}) = 180.5 \text{ K/W}$ ,  $\Delta T(\text{sapphire}) = 117.3 \text{ K}$ , and  $\Delta T(\text{GaN}) = 5.4 \text{ K}$ . Then the calculated temperature  $T_{\text{CHANNEL}}$  using our model on the top surface becomes  $176 \text{ }^\circ\text{C}$ . The measured value was  $180 \text{ }^\circ\text{C}$  and the 3-D model predicted  $140 \text{ }^\circ\text{C}$ . Hence our method again predicts the temperature more accurately.

### C. Multi-Finger GaN Device on SiC

An 8-gate device on SiC (fig. 1) for 2 to 4 GHz amplifier applications was measured in [23], and the thermal profile is shown in figure 7. Using the outlined procedure, one obtains  $T_{\text{CHANNEL}} = 183 \text{ }^\circ\text{C}$  (shown dotted); which agrees favorably with the average of the measurement. Notice our calculation only provides an average temperature on a given surface.

In general the channel temperature may be expressed as

$$T_{\text{CHANNEL}} = T_{\text{AMB}} + R_{TH}(T) P_{\text{SUPPLY}}(1 - PAE) \quad (14)$$

where  $T_{\text{AMB}}$  is the ambient (heat sink) temperature,  $R_{TH}(T)$  is the temperature dependent total thermal resistance of the stack, and  $PAE$  is the power added efficiency, which may be expressed as

$$PAE = \frac{\text{rf power developed}}{P_{\text{SUPPLY}}} \left( 1 - \frac{1}{G_p} \right) \quad (15)$$

where  $P_{\text{SUPPLY}}$  is the DC bias power, and  $G_p$  is the large signal power gain. Figure 8 gives the channel temperature for several cases of developed power density and values for  $PAE$ . Table 1 gives the thermal resistance breakdown for the layers that constitute the 8 gate device in figure 1. Observe that the highest thermal resistance is developed in the GaN layer.

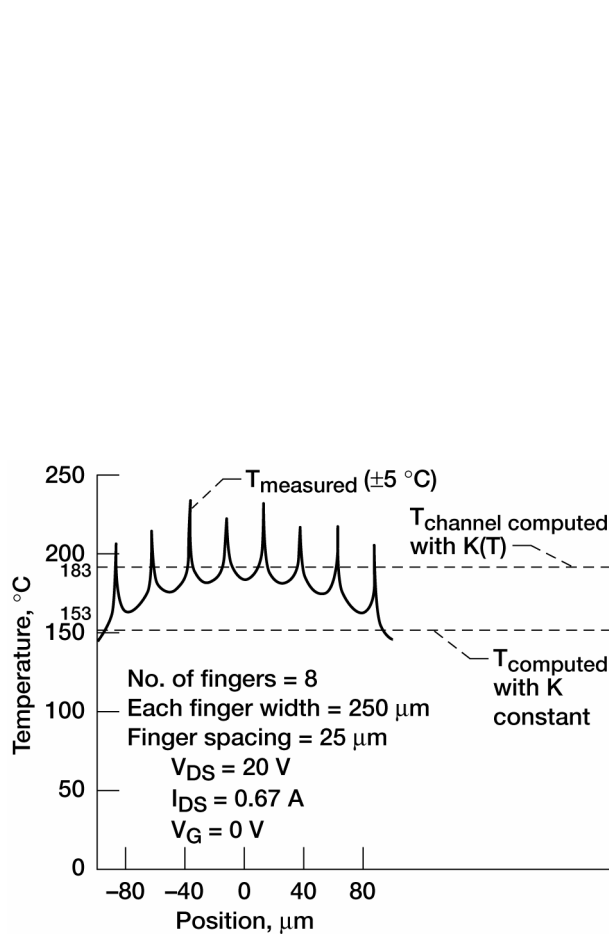


Figure 7.—Comparison of computed  $T_{\text{channel}}$  with measured temperature versus transverse position for an 8 gate AlGaIn/GaN HEMT of Kuball [23]. The measurement (solid) [23] data and computed (dotted) value.

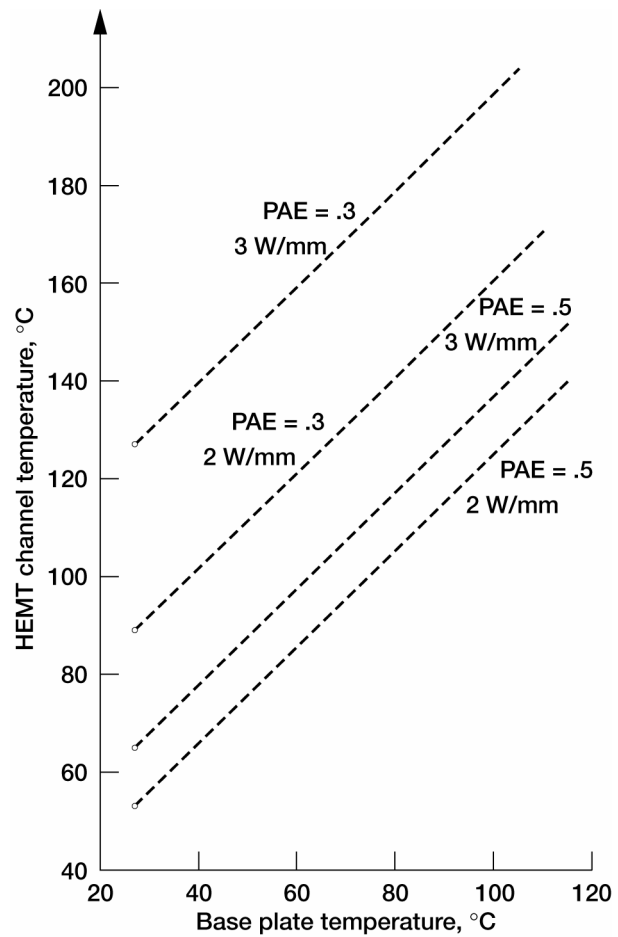


Figure 8.—Plot of computed channel temperature versus base plate (ambient) temperature for an 8 gate AlGaIn/GaN HEMT for several values of developed RF power (W/mm) and power added efficiencies (PAEs).

Table 1.—The change in channel temperature as the developed RF power and PAE are varied. This is for an 8 gate device,  $L_g = 0.15 \mu\text{m}$ ,  $W_g = 100 \mu\text{m}$ , gate centered in the source-drain gap of  $2 \mu\text{m}$ . RF power $\times$ eff. =  $P_{\text{DISS}}$

RF Power density, W/mm	PAE, percent	Carrier plate temperature, K (°C)	Channel temperature, K (°C)	Thermal resistance (°C/W)				
				$R_{\text{carrier plate}}$	$R_{\text{solder}}$	$R_{\text{SiC}}$	$R_{\text{AlN}}$	$R_{\text{GaN}}$
2	30	300 (27)	362 (89)	0.02	0.525	7.67	10.7	56.5
2	50	300 (27)	326 (53)	0.02	0.525	7.58	10.7	55.1
3	50	300 (27)	400 (127)	0.02	0.525	8.02	10.7	63.4
3	50	300 (27)	338 (65)	0.02	0.525	7.44	10.7	52.7

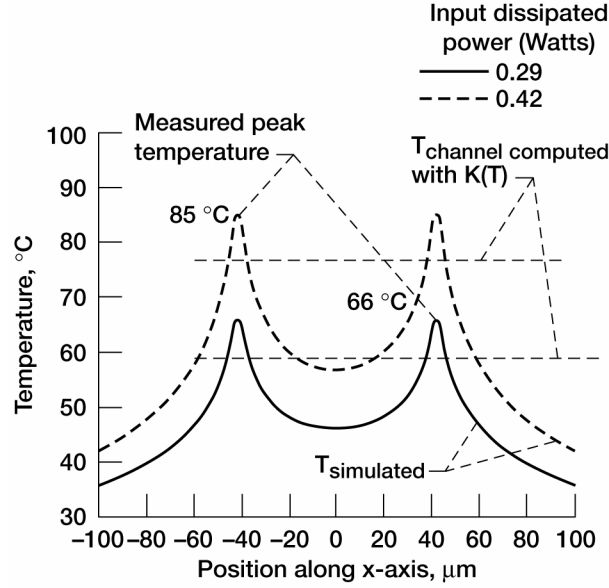


Figure 9.—Comparison of computed  $T_{\text{channel}}$  with measured peak and simulated temperature profile of Park [25], versus transverse position for a 2 gate device for two levels of input dissipated power.

#### D. Two-Finger GaN Device on Sapphire

Measurements using nematic liquid crystal thermography on a two-gate device on sapphire were performed in [25]; see figure 9. Our computations yielded  $T_{\text{CHANNEL}} = 59$  and  $76.5$  °C for the two input power dissipation levels  $P_{\text{DISS}}$ , respectively. Again the predicted values are near a rough visual average of the channel temperature.

Our modeling procedure can estimate the channel temperature to within 5 to 10 percent, and in some cases, much better than that.

#### IV. SSPA THERMAL MANAGEMENT ESTIMATE

Figure 10 is a hypothetical 50 W SSPA which consists of four MMIC chips, each of which develops 12.5 W, with 50 percent PAE, and they are combined by a lossless circuit. Each chip has 8 multi-gate amplifiers and each amplifier has 8 gate fingers. This implies the developed power density is  $1.95$  W/mm; which is a very reasonable and attainable value. The details of an amplifier on the MMIC are shown in figure 11(a). On the top surface the devices are about  $360$  μm long and separated  $410$  μm. At the heat sink their thermal footprints are about  $648 \times 388$  μm. The approximate heat spreading angles are shown dotted in figure 11(a), and the figure is not to scale. The thermal resistance stack is shown in figure 11(b), and the temperatures at the interfaces are given. Figure 11(c) is a cross-sectional view to demonstrate the approximate heat paths. The calculation proceeds as follows. In the GaN layer, the heat sources are sufficiently separated ( $\sim 40$  μm) so they may be treated as isolated regions. Thus the spreading angle is  $45^\circ$  and  $R_{TH}$  is  $63.4$  K/W using equation (7), or  $56.4$  K/W using equation (11). We assume the larger value is most accurate. The footprint at the GaN/AlN interface is  $1.15 \times 101$  μm and we estimate the spreading angle from [26]

$$\frac{\tan \theta_i}{\tan \theta_r} = \frac{\kappa_r}{\kappa_i} \quad (16)$$

where the angles are measured from the normal, and the subscripts  $i$  and  $r$  refer to the upper and lower layers respectively. This yields  $\theta_r = 3.6^\circ$ , so we can use the simple formula for  $R_{TH}$ , that is  $R_{TH} = l/(A\kappa)$  where  $l$  is the layer thickness and  $A$  is the cross-sectional area. We obtain  $R_{TH} = 12.9$  K/W. The footprint at the AlN/SiC boundary is  $1.152 \times 101 \mu\text{m}$  and we assume the  $40 \mu\text{m}$  separation for simplicity. This gives  $R_{TH} = 6.96$  K/W and spreading angle of  $64.8^\circ$ . This implies the fluxes intersect at about  $10 \mu\text{m}$  into the SiC layer. Assuming the final footprint at the AuSn-heatsink interface to be about  $388 \times 648 \mu\text{m}$  as in figure 11(c), the composite spreading angle is about  $59^\circ$ . The thermal cross-talk between adjacent regions is approximated using either [27] or [28], which yield  $\Delta T_{12} = 6.6$  or  $7.4$  K, respectively. Thus we choose the sink to be at  $67^\circ\text{C}$ . The temperatures at the interfaces are found next. Starting at  $T_1$ :  $T_1 = (1.5625 \text{ W})(0.937 \text{ K/W}) + 340 \text{ K} = 341.5 \text{ K}$ . The change in effective temperature across the SiC layer is  $(1.5625)(6.96 \text{ K/W}) = 10.9 \text{ K}$ , thus the effective temperature on the top surface of the SiC layer is  $T^e = 10.9 \text{ K} + 341.5 \text{ K} = 352 \text{ K}$ . Then  $T_A$  is  $352.2 \text{ K}$  using equation (15). Then  $T_3 = (1.5625/8)(12.9 \text{ K/W}) = 354.7 \text{ K}$ . The temperature change across the GaN layer is  $\Delta T = (1.5625/8)(63.4 \text{ K/W}) = 12.4 \text{ K}$ . Then the effective temperature on the top surface is  $T^e = 354.7 \text{ K} + 12.4 \text{ K} = 367.1 \text{ K}$ . Finally, the channel temperature is obtained as  $367.4 \text{ K}$  from equation (14). This value,  $94.4^\circ\text{C}$  is quite reasonable, and close to similar ones reported for similar devices.

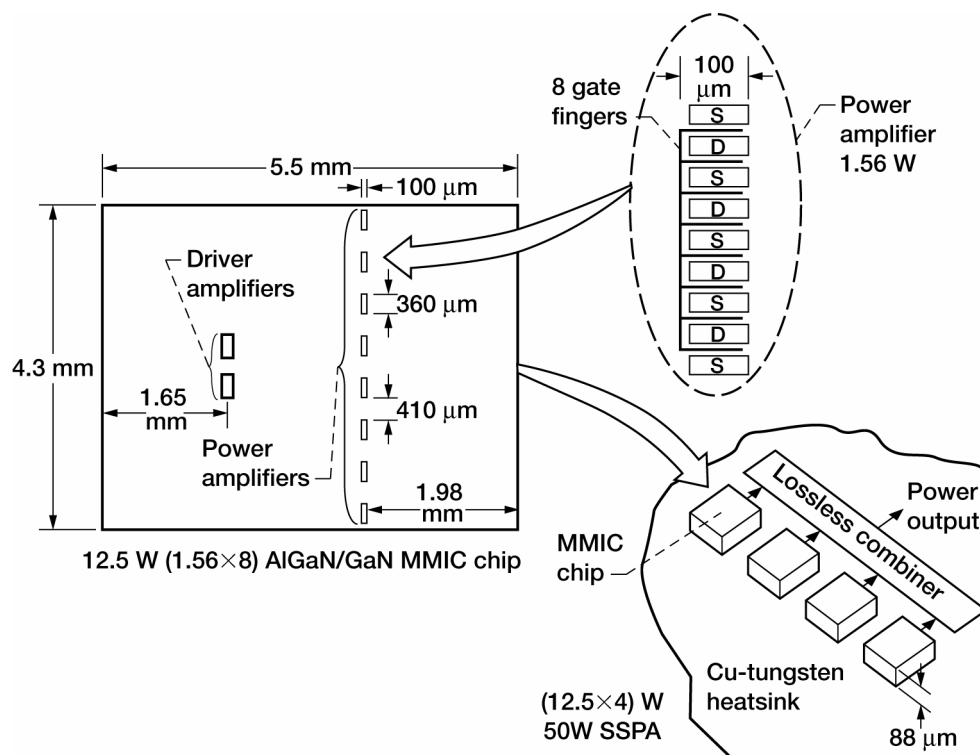


Figure 10.—Concept of a GaN MMIC chip with 8 amplifiers, and each amplifier consisting of 8 gates, each  $100 \mu\text{m}$  wide. The four chips are assumed to be soldered onto a Cu-tungsten heatsink, and combined to produce nearly 50 W.

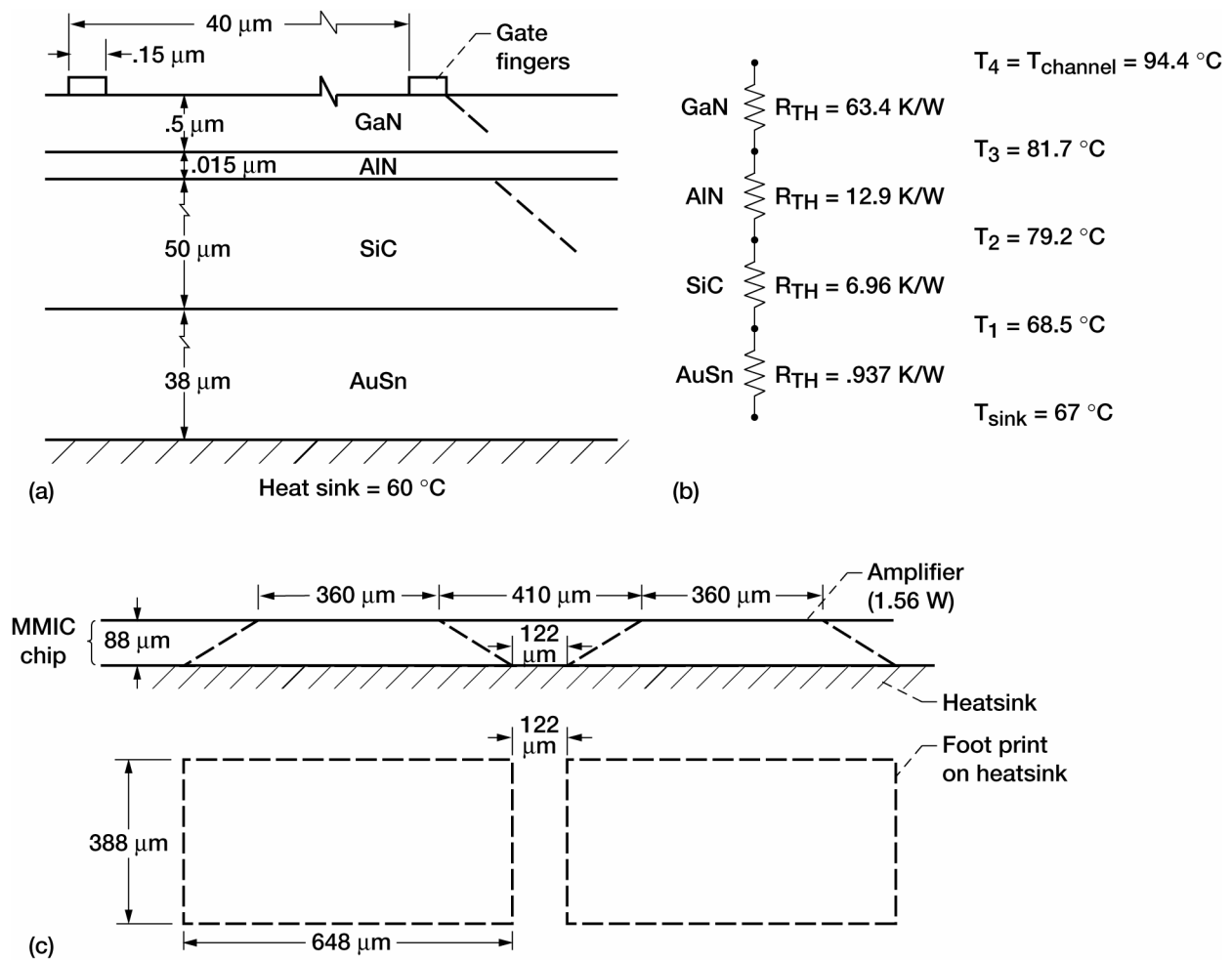


Figure 11.—(a) Cross-section and the approximate spreading angles into each layer. (b) Corresponding thermal resistance stack with the interface temperatures. (c) Effective footprints at the AuSn/Cu-tungsten heatsink interface, which shows the 59° effective spreading angle for the entire (composite) chip.

## V. CONCLUSIONS

We have demonstrated a simple analytical method to estimate the channel temperature in an AlGaN/GaN HEMT for microwave power amplifiers. It is applicable for multi-gate, multi-layer structures on SiC or Sapphire substrates, and for wide ranges of dissipated power. With accurate expressions for the temperature dependent thermal conductivity and using previously published equations for the thermal resistance of parallel stripes, one calculates a temperature that is within 5 to 10 percent of the true average channel temperature.



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